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FROM: Gregory W. Carr, Reg. No. 31,093

MESSAGE:

Pre-Appeal Brief Request for Review (9 pgs)
Notice of Appeal (1 pg)
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ATTORNEY DOCKET NO.
AUS920010797US1

PATENT APPLICATION
SERIAL NO. 10/042,103

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Allen et al.

Serial Number: 10/042,103

Filed: January 7, 2002

For: FIXED SNOOP RESPONSE TIME FOR SOURCE-CLOCKED MULTIPROCESSOR BUSSES

Group Art Unit: 2143

Examiner: Jude Jean Gilles

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reasons stated on the attached sheets.

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REMARKS

Applicants respectfully request review of the final rejection in this case for the following reasons. The Examiner has omitted several essential elements needed for a prima facie rejection in offering a combination that does not include each and every element of the Claims and contradicts more than one element of the Claims. Briefly, the Examiner's proposed combination introduces signal delay at a transmitter, while the claimed embodiments introduce signal delay at a receiver. Further, the Examiner's proposed combination does not include other elements, such as, for example, multiple clocks, multiple (and different) delay times, and other elements.

Claims 1-20 stand rejected under 35 U.S.C. §103(a) by U.S. Patent No. 5,555,382 by Thaller et al. ("Thaller") in view of U.S. Patent No. 6,070,205 by Kato et al. ("Kato"), further in view of U.S. Patent No. 6,754,838 B2 by Burns et al. ("Burns"). Regarding Claim 1, the Examiner offered Thaller as allegedly providing the bulk of the limitations, admitting that "Thaller does not teach in detail a second microprocessor connected to the memory controller through at least a second bus for transmitting at least a second signal from the memory controller to the second processor, the second bus requiring a first period of time more to transmit the second signal than what the first bus requires to transmit the first signal, the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time." Final Action dated Oct. 20, 2005, Page 4.

The Examiner offered Burns as teaching, "a system capable of transmitting data to a plurality of processors generating two clock signals, the length of which when traced differ by the amount of tuning etch required to add sufficient delay to the forwarded clock signals transmitted to the processors." Final Action dated Oct. 20, 2005, Pages 4-5. The Examiner's proposed

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combination, which was alleged to teach each and every element of Claim 1, "incorporated Kato' [sic] teaching a second microprocessor connected to the memory controller, ***with the clock signals of Burns generating the delay***, with the teachings of Thaller. . ." Final Action dated Oct. 20, 2005, Page 5 (emphasis added).

Accordingly, the Examiner expressly employs the Burns clock-forwarding scheme in the proposed combination. In the Burns scheme, "delay in the forwarded clock signal is generated *at the transmitting device* by adding tuning etch," (Burns, Abstract, emphasis added) with "the major advantage of [the Burns] technique is that it *eliminates the need to insert tuning etch upstream* to the forwarded clock signal associated with each individual data bundle." Burns, col. 7, lines 6-8 (emphasis added).

In the present invention, the *receiving end* of a first bus signal on a first unidirectional point-to-point bus delays the first bus signal while a second bus signal on a second unidirectional point-to-point bus is transmitted to a *different* receiver. That is, the bus transaction *destination* module delays a signal. As recited in Claim 1, for example, "the first interfacing logic [of the first microprocessor] delay[s] the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time." The first signal is transmitted "from the memory controller" (the transmitting device) "to the first interfacing logic" (the receiving device), as recited in Claim 1.

Not only does Burns not disclose the same method or system for delaying a signal as the present invention, Burns teaches generating a delay *at the transmitting device*, affirmatively teaching away from the present invention. As described above, Claim 1 recites "the first interfacing logic delaying the first signal," where the first microprocessor includes the first interfacing logic and

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the first bus transmits "at least a first signal from the memory controller to the first interfacing logic."

As described above, the Examiner admits that this limitation is absent in Thaller, and expressly offers Burns to supply this limitation. Burns clearly does not teach the limitations as claimed, and in fact teaches away from the limitations as claimed. Not only has the Examiner failed to show a prima facie obviousness combination, the combination he does offer expressly teaches away from the claimed limitations. This constitutes a clear error on the part of the Examiner and requires reversal.

Moreover, the Examiner also expressly applies the exact same fatally-flawed combination to Claims 2-18. "The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 2." Final Action dated Oct. 20, 2005, Page 6. "The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 3." Final Action dated Oct. 20, 2005, Page 6. "The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 4." Final Action dated Oct. 20, 2005, Page 6. "The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 10." Final Action dated Oct. 20, 2005, Page 13. The Examiner includes that same sentence, expressly adopting his erroneous combination, in each of his rejections of Claims 2-10. The Examiner also rejects Claims 11-18 as "substantially the same as" Claims 2-9, respectively. *See* Final Action dated Oct. 20, 2005, Page 16.

Claims 2-9 depend on and further limit Claim 1. Claims 11-18 depend on and further limit Claim 10. Thus, given that Applicants have shown that at least one essential element required for a prima facie obviousness case is missing as to Claims 1 and 10, that same element is also missing as

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to the dependent claims. Accordingly, Applicants respectfully request that the rejections against Claims 1-18 be withdrawn and that Claims 1-18 be allowed.

Regarding Claims 19 and 20, the Examiner does not expressly state that he is using the Burns clock-forwarding scheme to provide any particular limitation. Instead, the Examiner states, "the combination Thaller-Kato-Burns teaches a system, comprising," followed by a recitation of the claim limitations with citations to one or more of the references. *See* Final Action dated Oct. 20, 2005, Pages 13-15.

Claim 19 includes the limitation, "wherein the first interfacing logic is configured to delay the first signal by a second period of time and the second interfacing logic is configured to delay the second signal by a third period of time so that the first signal and the second signal are respectively received by the first microprocessor and the second microprocessor substantially at the same time." In the Examiner's recitation of the elements of Claim 19, for this limitation, the Examiner cites, "[see *Burns, fig. 4, items 300, 100a-b, 8, 370, 390; column 6, lines 28-67; column 7, lines 1-44*]." Final Action dated Oct. 20, 2005, Page 14. The Examiner also provides this citation for a corresponding limitation of Claim 20. *See* Final Action dated Oct. 20, 2005, Page 15.

This is the exact same citation the Examiner provided with respect to this element in the Examiner's rejection of Claim 1. *See* Final Action dated Oct. 20, 2005, Page 5. Accordingly, Applicants respectfully submit that the Examiner is in fact employing the same rationale to reject Claims 19 and 20 as he employed to reject Claims 1-18, even if that rationale is not express.

As such, the Examiner's proposed combination is as fatally flawed as applied to Claims 19 and 20 as it is against Claims 1-18. Namely, the Examiner's proposed combination provides for introducing delay at the transmitter-side of a unidirectional bus, while the claimed embodiments introduce delay at the receiver-side of a unidirectional bus.

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Thus, given that Applicants have shown that at least one essential element required for a prima facie obviousness case is missing as to Claims 19 and 20, Applicants have shown that the rejections of Claims 19 and 20 constitute clear error on the part of the Examiner. Accordingly, Applicants respectfully request that the rejections against Claims 19 and 20 be withdrawn and that Claims 19 and 20 be allowed.

In addition to the above-described limitations, there are also other essential elements missing from the Examiner's proposed combination. For example, the Examiner's proposed combination also fails to show multiple clocks, multiple delay times, and other elements. Regarding Claim 1, the Examiner cites Thaller as showing, "the memory controller being clocked by a second system clock." Final Action dated Oct. 20, 2005, Page 3. But, as described above, the Examiner also expressly relies on Burns to supply the clock signals in the Examiner's proposed combination. Further, no matter which clock signals the Examiner selects for the proposed combination, Thaller's or Burns', neither reference actually shows "the memory controller being clocked by a second system clock."

Instead, Thaller shows two CPU modules, each of which is equipped with a clock subsystem, but only one clock is active at any one time: "While each of the two CPU modules 14, 16, contain bus clock subsystems 260, only the clock subsystem 260 on the primary CPU module 14 is enabled." Thaller, col. 7, lines 43-45. Thus, Thaller does not show "the memory controller being clocked by a second system clock."

Nor does Burns show "the memory controller being clocked by a second system clock." Instead, Burns teaches generating two forwarded clock signals for transmission with data. "A common clock source 340 is used to generate two clock signals: FWDCLKOUT and DATACLKOUT." Burns, col. 6, lines 47-49. These clock signals are "tuned," eventually making

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their way off-chip with a data stream, "The delayed clock signals CLOCK1 and CLOCK2 are then transmitted with the data to the destination devices 100a, 100b." Burns, col. 7, lines 2-4.

Claim 1, however, recites, "a first microprocessor . . .being clocked by a first system clock" and "a memory controller . . .being clocked by a second system clock." Clearly, in the Burns configuration, the clock signals are closely tied to each other and to the transmitted data, while in the embodiment recited in Claim 1, the first microprocessor and the memory controller are clocked by independent clocks. Therefore, the Examiner's proposed combination lacks yet another essential limitation.

And regarding Claim 19, the failure of the Thaller/Burns clocks is even more apparent, as Claim 19 recites, "the second microprocessor being clocked by a third system clock." Notwithstanding the above showing that Thaller/Burns fails to teach a second system clock, there is absolutely nothing in any of the Examiner's cited references to support a *third* clock.

Nor does the Examiner' proposed combination support multiple delay times as recited in the Claims. The Examiner admits that Thaller does not show, among other things, "delaying the first signal by the first period of time." Final Action dated Oct. 20, 2005, Page 4. Nowhere does the Examiner's proposed combination show, for example, "delaying the second signal by a third period of time" as recited in Claim 4, or "delay[ing] the second signal by a third period of time" as recited in Claim 19. These and other essential elements are plainly missing from the Examiner's proposed combination. However, given that the Examiner's proposed combination clearly fails to teach each and every element, as described above, the remaining missing elements are cumulative to the Applicants argument and are reserved.

Therefore, in light of the foregoing remarks, demonstrating that the Examiner has omitted at least two essential elements from the Examiner's proposed combination, Applicants respectfully

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submit that the Examiner has failed to present a prima facie case for obviousness. Further, this failure constitutes a clear error. Applicants therefore respectfully request that the rejections against Claims 1-20 under 35 U.S.C. §103(a) be withdrawn and that Claims 1-20 be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-20.

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AUS920010797US1

PATENT APPLICATION
SERIAL NO. 10/042,103

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Respectfully submitted,

CARR LLP

Dated: 3/13/06

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